(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 September 2005 (01.09.2005)

PCT

(10) International Publication Number
WO 2005/081449 A1

(51) International Patent Classification[7]: H04L 7/00

(21) International Application Number:
PCT/US2004/002913

(22) International Filing Date: 2 February 2004 (02.02.2004)

(25) Filing Language: English

(26) Publication Language: English

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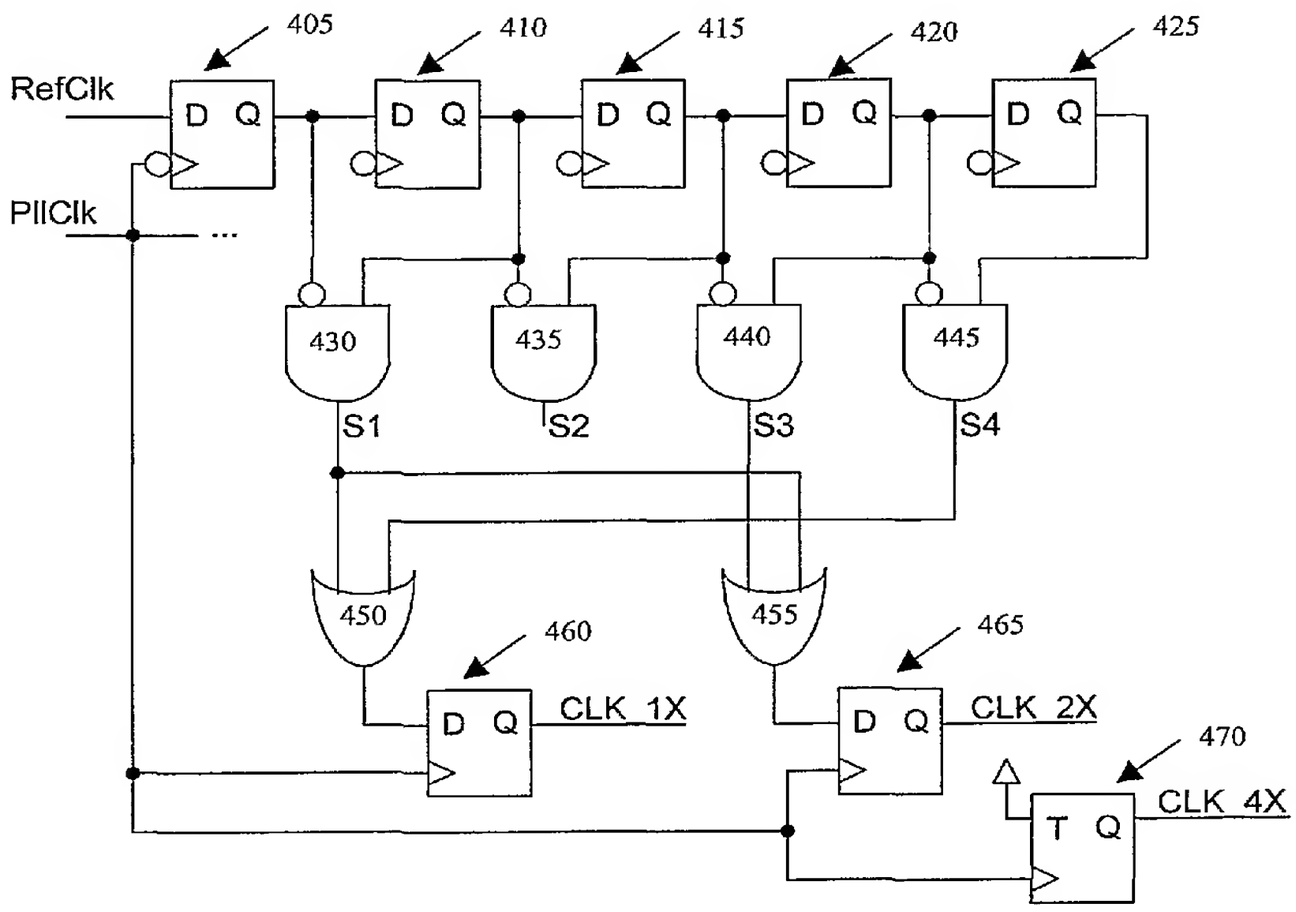
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**
— *with international search report*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: ANALOG TO DIGITAL CONVERTER CLOCK SYNCHRONIZER




(57) Abstract: The present application generally relates to apparatuses such as television signal processing apparatus that process radio frequency signals. More specifically, the present application is particularly useful in integrated circuits that must receive a radio frequency signal and simultaneously use circuitry where the timing of the operations are based on the received RF signal and circuitry where the timing is based on a fixed rate signal with sensitivity to clock jitter. According to an exemplary embodiment, the apparatus comprises, a first input (RefClk), a second input (PllClk), an output (CLK 1X), a delay means (405, 410, 415, 420, 425), and a logic means (430, 435, 440, 445, 450, 455, 460, 465, and 470) to compare a plurality of stages of said delay means to produce an signal at said output.

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